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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/768,665
Filing Date: January 24, 2001
Appellant(s): NGUYEN ET AL.

Roger Fulghum
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 10/03/2007 appealing from the Office action mailed 12/27/2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,282,601	GOODMAN ET AL	8-2001
3,643,227	SMITH ET AL	2-1972

Applicants' Admitted Prior Art, page 1, line 14 to page 3, line 21.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 4-8, 16, and 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Goodman et al. (U.S. Patent No. 6,282,601) and Smith et al. (U.S. Patent No. 3,643,227).

Referring to claim 1: The admitted prior art discloses writing parameters for the SMI routines to a predetermined register of a first processor (Specification, page 3, lines 4-6), executing in the first processor a command of a software application to cause the first processor to initiate a system management interrupt (Specification, page 2, lines 8-

17), receiving at each processor an instruction that the system management interrupt has been issued (Specification, page 2, lines 19-20), entering system management mode at each processor (Specification, page 2, lines 20-21), and saving register contents of each processor to a memory space associated with each respective processor (Specification, page 2, lines 22-24). The admitted prior art's parameters for the SMI routines are the claimed predetermined signature.

The admitted prior art further discloses that a different processor, other than the processor initiating the interrupt, may be selected for handling the interrupt (Specification, page 3, lines 13-16); thus, the admitted prior art discloses selecting from among the multiple processors a second processor as a system management interrupt handler. **Note that to select is to choose in preference to another or others. Note also that selection must be based on specific criteria. Thus, it is clear that selection based on specific criteria is selection based on an arbitration scheme. In any event, as already indicated by Ex. King, the use of arbitration scheme in general is old and well-known as evidenced by at least Smith.**

Neither the admitted prior art discloses selecting the second processor according to an arbitration scheme nor the admitted prior art discloses scanning the content of the memory for the selected second processor to process the interrupt.

Goodman discloses an interrupt handling method in a multiprocessor environment. Goodman discloses scanning the content of the memory for the selected second processor to process the interrupt (figure 4, steps 126, 128, and 130); and when the second processor locates the saved predetermined signature in one of the memory

spaces associated with the processors of the computers system, using the contents of the memory space associated with the predetermined signature for any parameters necessary for the handling of the system management interrupt (figure 4, steps 134, 136, and 138). Goodman teaches one to identify the requesting processor without having to satisfy severe interrupt timing constraint (column 1, lines 66-67, column 2, lines 1-5). Although Goodman discloses and teaches one to scan the processor register in handling interrupt, Goodman does not explicitly disclose an arbitration scheme in selecting one processor to execute the interrupt.

Smith discloses assigning tasks to the idle processor (abstract). Smith teaches one to distribute the task to the processor based on the processor's current workload.

Hence, it would have been obvious to one having ordinary skill in the computer art to adapt the teachings of Goodman and Smith onto the admitted prior art because Goodman teaches one to identify the requesting processor without having to satisfy severe interrupt timing constraint and Smith teaches one to balance each processor's workload by distributing the task according to the processor's current workload.

Referring to claim 4: Claim 1's argument applies; furthermore, since Smith teaches one to select the processor based on the workload; it can be any processor, including the one just causes the SMI.

Referring to claim 5: The admitted prior art discloses the processors' access to chip set's I/O port as one standard well-known system activities (Application, page 3, lines 8-9). Goodman also discloses that the processor writes to the memory (figure 1, structure 26) via the chip set's port (figure 1, structure 18).

Referring to claims 6-7: Both the admitted prior art (Specification, page 2, line 11) and Goodman (figure 1, structure 50) disclose the chip sets as a PCI bridge.

Referring to claim 8: The admitted prior art discloses the step of issuing from the expansion bridge the instruction causing the processor to enter the system management mode (Specification, page 2, lines 10-17). Goodman discloses that each of the processors of the system to enter system management mode (column 1, lines 50-54).

Referring to claim 16: The admitted prior art discloses issuing an instruction from a first processor of the system to a chip set (Specification, page 2, lines 10-11), receiving the instruction at the chip set and in response issuing a command causing the processors to enter system management mode (Specification, page 2, lines 12 and 18-19), writing parameters for the SMI routines to a predetermined register of a first processor (Specification, page 3, lines 4-6), and saving register contents of each processor to a memory space associated with each respective processor (Specification, page 2, lines 22-24). The admitted prior art's parameters for the SMI routines are the claimed predetermined signature.

The admitted prior art further discloses that a different processor, other than the processor initiating the interrupt, may be selected for handling the interrupt (Specification, page 3, lines 13-16); thus, the admitted prior art discloses selecting from among the multiple processors a second processor as a system management interrupt handler and then transmitting the software system management interrupt to the selected second processor.

Neither the admitted prior art discloses selecting the second processor according to an arbitration scheme nor the admitted prior art discloses scanning the content of the memory for the selected second processor to process the interrupt.

Goodman discloses an interrupt handling method in a multiprocessor environment. Goodman discloses scanning the content of the memory for the selected second processor to process the interrupt (figure 4, steps 126, 128, and 130); and when the second processor locates the saved predetermined signature in one of the memory spaces associated with the processors of the computers system, using the contents of the memory space associated with the predetermined signature for any parameters necessary for the handling of the system management interrupt (figure 4, steps 134, 136, and 138). Goodman teaches one to identify the requesting processor without having to satisfy severe interrupt timing constraint (column 1, lines 66-67, column 2, lines 1-5). Although Goodman discloses and teaches one to scan the processor register in handling interrupt, Goodman does not explicitly disclose an arbitration scheme in selecting one processor to execute the interrupt.

Smith discloses assigning tasks to the idle processor (abstract). Smith teaches one to distribute the task to the processor based on the processor's current workload.

Hence, it would have been obvious to one having ordinary skill in the computer art to adapt the teachings of Goodman and Smith onto the admitted prior art because Goodman teaches one to identify the requesting processor without having to satisfy severe interrupt timing constraint and Smith teaches one to balance each processor's workload by distributing the task according to the processor's current workload.

Referring to claim 19: The admitted prior art discloses the processors' access to chip set's I/O port as one standard well-known system activities (Application, page 3, lines 8-9). Goodman also discloses that the processor writes to the memory (figure 1, structure 26) via the chip set's port (figure 1, structure 18).

Referring to claims 20-21: Both the admitted prior art (Specification, page 2, line 11) and Goodman (figure 1, structure 50) disclose the chip sets as a PCI bridge.

Referring to claims 22-23: The admitted prior art discloses receiving at each processor an instruction that the system management interrupt has been issued (Specification, page 2, lines 19-20) and entering system management mode at each processor (Specification, page 2, lines 20-21).

The admitted prior art further discloses that a different processor, other than the processor initiating the interrupt, may be selected for handling the interrupt (Specification, page 3, lines 13-16); thus, the admitted prior art discloses selecting from among the multiple processors a second processor as a system management interrupt handler.

But the admitted prior art does not disclose selecting the second processor according to an arbitration scheme. The admitted prior art also does not disclose scanning, locating, and retrieving the content of the memory for the selected second processor to process the interrupt.

Goodman discloses an interrupt handling method in a multiprocessor environment. Goodman discloses scanning the contents of the memory space associated with each processor (figure 4, steps 126, 128, and 130); and when the

second processor locates the saved predetermined signature in one of the memory spaces associated with the processors of the computers system, using the contents of the memory space associated with the predetermined signature for any parameters necessary for the handling of the system management interrupt (figure 4, steps 134, 136, and 138). Goodman teaches one to identify the requesting processor without having to satisfy severe interrupt timing constraint (column 1, lines 66-67, column 2, lines 1-5). Although Goodman discloses and teaches one to select a processor to handle the interrupt, Goodman does not explicitly disclose an arbitration scheme in selecting the processor.

Smith discloses assigning tasks to the idle processor (abstract). Smith teaches one to distribute the task to the processor based on the processor's current workload.

Hence, it would have been obvious to one having ordinary skill in the computer art to adapt the teachings of Goodman and Smith onto the admitted prior art because Goodman teaches one to identify the requesting processor without having to satisfy severe interrupt timing constraint and Smith teaches one to balance each processor's workload by distributing the task according to the processor's current workload.

(10) Response to Argument

With regard to claims 1, 14, and 16, Appellants argued that "Goodman teaches away from the claimed invention by expressly providing that all system management interrupts are to be handled by a single, dedicated processor. Goodman plainly discloses that "only the boot processor" is to be involved in handling system

management interrupts (column 4, line 57). There is no teaching from Goodman to suggest that any processor other than the single boot processor is operable to handle a system management interrupt. Nowhere does Goodman suggest that multiple processors could be used to handle system management interrupts, as explicitly claimed in the present application. A plain reading of Goodman would lead a person of ordinary skill to conclude that only a single, dedicated processor is responsible for handling a system management interrupt, in direct contrast to the claims of the present invention."

In response to Applicants' argument, while the Examiner agrees with Applicants that Goodman discloses dedicating the boot processor to handle the interrupt management, Applicants are reminded that the rejection is based on a combination of references. One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Goodman is relied upon in the above 103 Rejection as Goodman discloses an interrupt handling method in a multiprocessor environment. Goodman discloses scanning the contents of the memory space associated with each processor (figure 4, steps 126, 128, and 130); and when the second processor locates the saved predetermined signature in one of the memory spaces associated with the processors of the computers system, using the contents of the memory space associated with the predetermined signature for any parameters necessary for the handling of the system management interrupt (figure 4, steps 134, 136, and 138).

Goodman teaches one to identify the requesting processor without having to satisfy severe interrupt timing constraint (column 1, lines 66-67, column 2, lines 1-5).

Appellants also argued that "when considering the teachings of Goodman as a whole, a person of ordinary skill would be encouraged to use only a single, dedicated processor as the processor responsible for handling a system management interrupt. When considered as a whole, the prior art counsels directly against Appellants' invention. This is 'strong evidence' of the nonobviousness of the invention because Goodman teaches a solution that is the opposite of the invention of the present application. '[M]atter in the prior art which counsels against doing what the inventor did is strong evidence that the inventor's solution is not obvious.' Johnson & Son, Inc. v. Gillette Co., 1989 WL 87374, *42, Civ. A. Nos. 83-2657-N, 83-3201-N, (D. Mass. 1989). Therefore, Appellants respectfully submit that Goodman must be considered in its entirety, and, when Goodman is considered in its entirety, Goodman teaches away from the claimed invention. As a result, a rejection of the pending claims on the basis of any combination involving Goodman is improper, and for this reason alone, a prima facie case of obviousness has not been established."

Contrary to Appellants' argument, Goodman does not teach away from Appellants' invention. **It is important for Appellants to recognize what is taught by Goodman and is also used to formulate the above 103 Rejection.** As already noted above, Goodman is relied upon in the above 103 Rejection as Goodman discloses an interrupt handling method in a multiprocessor environment. Goodman discloses scanning the contents of the memory space associated with each processor (figure 4,

steps 126, 128, and 130); and when the second processor locates the saved predetermined signature in one of the memory spaces associated with the processors of the computers system, using the contents of the memory space associated with the predetermined signature for any parameters necessary for the handling of the system management interrupt (figure 4, steps 134, 136, and 138). Goodman teaches one to identify the requesting processor without having to satisfy severe interrupt timing constraint (column 1, lines 66-67, column 2, lines 1-5). **Goodman DOES NOT relied upon in the above 103 Rejection for the teaching of a "single, dedicated processor as the processor responsible for handling a system management interrupt" (see Appellants' argument above).**

As clearly set forth in the above 103 Rejection, the problem to be solved is the interrupt timing constraint in multi-processor system regardless of whether one of the processor in the multi-processor system is dedicated to interrupt processing or none of the processors in the multi-processor system is dedicated for interrupt processing (any processor in a multi-processors can process interrupts). Goodman provides a solution to the exact problem of severe interrupt timing constraint (column 1, lines 66-67 and column 2, lines 1-5) by scanning the contents of the memory space associated with each processor, and using the contents of the memory space associated with the predetermined signature for any parameters necessary for the handling of the system management interrupt. In other words, the teaching of Goodman, not only beneficially used to solve the problem of severe interrupt timing constraint in a multi-processor system, wherein one processor is dedicated to interrupt processing, but also can be

used in multi-processor system, wherein none of the processors is dedicated for interrupt processing (any processor can process interrupts). It is also noted that Appellants have not provided any evidence or even argument to show that the teaching of Goodman cannot be used in the admitted prior art.

Thus, it is clear from discussion above that Goodman does not teach way from the invention as alleged by Appellants.

In addition, Appellants argued that "Goodman, taken alone or in combination with Smith and Applicants' allegedly admitted prior art, does not teach or suggest all of the claim limitations of the present invention. Namely, because Goodman teaches a single, dedicated processor responsible for handling a system management interrupt, Goodman fails to teach or suggest that each processor of the multiple processors is operable to process a system management interrupt and none of the processors are dedicated to processing system management interrupts. Additionally, Applicants' allegedly admitted prior art fails to remedy this deficiency, as the cited portions of the Background of Appellants' Specification discuss how, in a multi-processor system, a second processor may be unable to properly process a system management interrupt. (Specification, p.4, lines 18-22) Finally, Smith also fails to remedy the deficiencies of Goodman and Applicants' allegedly admitted prior art, as Smith fails to even discuss system interrupts. Thus, because the combination of references fails to teach or suggest all of the claim limitations of the present invention, a prima facie case of obviousness has not been established."

Contrary to Appellants' argument, as already discussed above, the rejection is based on a combination of references. Specifically, claims 1, 4-8, 16, and 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Goodman et al. (U.S. Patent No. 6,282,601) and Smith et al. (U.S. Patent No. 3,643,227). One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Khanh Dang
Primary Examiner

Conferees:

Mark Rinehart

Robert Beausoliel

(Notice of Panel Decision from Pre-Appeal Brief Review is hereby attached)

Application Number	Application/Control No.	Applicant(s)/Patent under Reexamination	
	09/768,665	NGUYEN ET AL.	
	Dang Khanh	Art Unit 2111	

Document Code - AP.PRE.DEC

Notice of Panel Decision from Pre-Appeal Brief Review

This is in response to the Pre-Appeal Brief Request for Review filed 06/04/07.

1. ☐ **Improper Request** – The Request is improper and a conference will not be held for the following reason(s):

   ☐ The Notice of Appeal has not been filed concurrent with the Pre-Appeal Brief Request.
   ☐ The request does not include reasons why a review is appropriate.
   ☐ A proposed amendment is included with the Pre-Appeal Brief request.
   ☐ Other:

The time period for filing a response continues to run from the receipt date of the Notice of Appeal or from the mail date of the last Office communication, if no Notice of Appeal has been received.

2. ☒ **Proceed to Board of Patent Appeals and Interferences** – A Pre-Appeal Brief conference has been held. The application remains under appeal because there is at least one actual issue for appeal. Applicant is required to submit an appeal brief in accordance with 37 CFR 41.37. The time period for filing an appeal brief will be reset to be one month from mailing this decision, or the balance of the two-month time period running from the receipt of the notice of appeal, whichever is greater. Further, the time period for filing of the appeal brief is extendible under 37 CFR 1.136 based upon the mail date of this decision or the receipt date of the notice of appeal, as applicable.

   ☒ The panel has determined the status of the claim(s) is as follows:
   Claim(s) allowed: *none*.
   Claim(s) objected to: *none*.
   Claim(s) rejected: *1, 4-8, 16, 19-23*.
   Claim(s) withdrawn from consideration: _____.

3. ☐ **Allowable application** – A conference has been held. The rejection is withdrawn and a Notice of Allowance will be mailed. Prosecution on the merits remains closed. No further action is required by applicant at this time.

4. ☐ **Reopen Prosecution** – A conference has been held. The rejection is withdrawn and a new Office action will be mailed. No further action is required by applicant at this time.

All participants:

(1) *Dang Khanh*.

(2) *Mark Rinehart*.

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(3) *Robert Beausoliel*.

(4)_____.